Abstract

The present invention is directed to determining the timing for a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths. Predictions are formed for timing delays in said signal paths in the integrated circuit. A first such path is selected, wires are traced in the integrated circuit forming the path, hereinafter referred to as victim wires, and adjacent and crossing wires thereto, hereinafter referred to as aggressor wires, are determined. For each aggressor wire, the amount of electromagnetic coupling to the victim wires of the first path is determined. The aggressor wires are divided into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires. A user is allowed to select a mode of operation, and for each victim wire, the timing delay predictions are modified based on the effects of the aggressor wires only in those categories corresponding to the mode of operation selected by the user.